9308

MSI DUAL FOUR-BIT LATCH

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTμL technology and is CCSL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

FEATURES

- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage (D.C.) (See Note 1)	−0.5 V to +5.5 V
Input Current (D.C.) (See Note 1)	−30 mA to +5 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

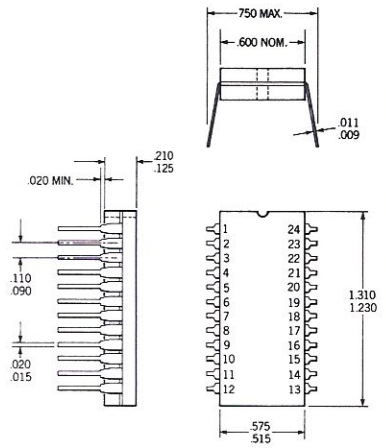
NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DESCRIPTION OF LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

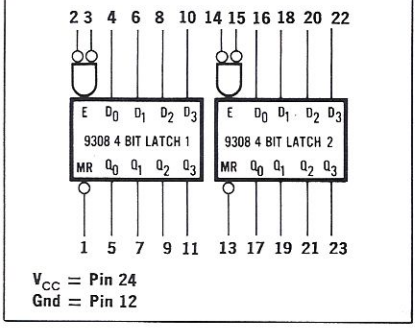
The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

ORDER INFORMATION — Specify U6N9308XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

Electrical Characteristics on Page 2.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, See Note 1) (Part #U6N930851X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 14.4\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 11.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1 and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_1 and MR Inputs				10	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

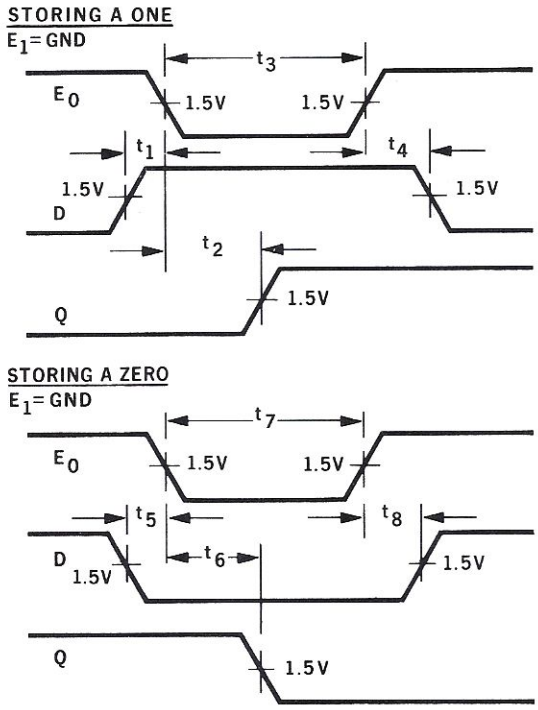
TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$, See Note 1) (Part #U6N930859X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OUT} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OUT} = 14.4\ mA$ $V_{CC} = 4.75\ V$, $I_{OUT} = 12.7\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1 and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_1 and MR Inputs				10	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

NOTE 1: Units are pulse tested.
NOTE 2: Output Voltages are guaranteed for either the input enabled or input disabled case.
NOTE 3: This current is measured at $V_{IN} = 0.0\ V$ to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.4\ V$ is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4) MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before the enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

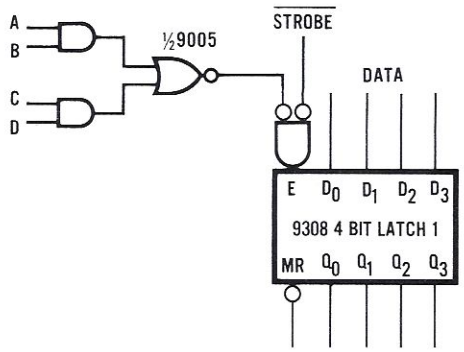
NOTE 4: Limits indicated by X will be shown on final data sheets.

All delays are measured with $V_{CC} = 5.0$ V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

LOADING RULES

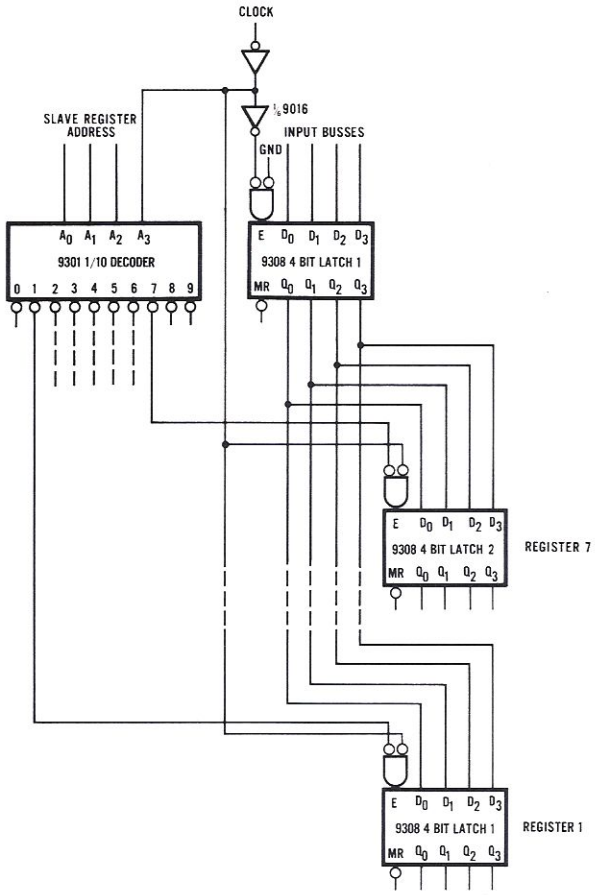
	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3	1.5
	MR, E_0, E_1	1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

APPLICATIONS

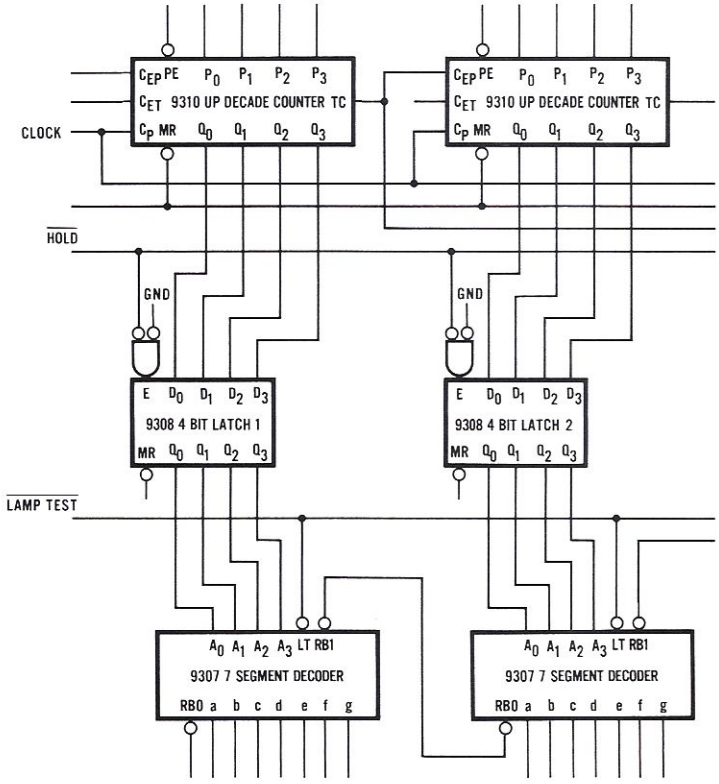


AND-OR ENABLE SHOWING ACTIVE LEVEL LOW ENABLE GATE UTILITY

SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP



9308 AS A HOLDING REGISTER IN COUNTING AND DISPLAY APPLICATIONS


CEP PE P0 P1 P2 P3
CET 9310 UP DECADE COUNTER TC
CP MR Q0 Q1 Q2 Q3
CLOCK
HOLD
GND
GND
E D0 D1 D2 D3
9308 4 BIT LATCH 1
MR Q0 Q1 Q2 Q3
E D0 D1 D2 D3
9308 4 BIT LATCH 2
MR Q0 Q1 Q2 Q3
LAMP TEST
A0 A1 A2 A3 LT RBI
9307 7 SEGMENT DECODER
RBO a b c d e f g
A0 A1 A2 A3 LT RBI
9307 7 SEGMENT DECODER
RBO a b c d e f g

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